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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/862,484	05/23/2001	Feng-Ting Pai	0941-0261P-SP	8958

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EXAMINER	
SHAPIRO, LEONID	

ART UNIT	PAPER NUMBER
2673	

DATE MAILED: 12/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/862,484	PAI ET AL.	
	Examiner	Art Unit	
	Leonid Shapiro	2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 July 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,6 and 7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,6 and 7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-2 and 6-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Admitted Prior Art (APA) in view of Herman (US Patent No. 4,325,063) and Taguchi et al. (US Patent No. 6.181.317 B1).

As to claim 1, APA teaches a method of processing signals of a timing controller of a liquid crystal display module, comprising the steps of:

(a) receiving a vertical synchronizing signal (See Fig. 3-4, items VSYNC, in description See from page 1, Line 27 to page 2, Line 6);

(b) receiving a data enable signal DE which has a vertical blank period (See Fig. 3-4, items DE, VB, in description See from page 1, Line 27 to page 2, Line 6);

© generating a gate clock signal CPV which has a plurality gate clock cycles C1-Cn (See Fig. 3-6, item CPV, in description See page 2, Lines 4-24);

(d) after a rising edge or a falling edge of the vertical synchronizing signal generating a plurality of gate-on enable signals OE simultaneously according to the plurality of gate clock cycles C1-Cn of gate clock CPV (See Fig. 3-6, item OE, in description See page 2, Lines 4-24);

(e) wherein the start vertical signals STV includes a first start vertical signal STV1 to determine a start scan location of a frame; and a second start vertical signal STV2 to offset flicker and display brightness of the liquid crystal display (See Fig. 3-6, items STV1, STV2, in description See page 2, Lines 4-6).

APA does not show after a rising edge or a falling edge of the vertical synchronizing signal generating start vertical signals STV before the end of the vertical blank period VB after at least a gate clock cycle C1 during vertical blank period VB.

Taguchi et al. teaches after a rising edge or a falling edge of the vertical synchronizing signal (See Fig. 12, item C-SYNC) generating start vertical signals STV (See Fig. 12, item STV (IN)) before the end of the vertical blank period VB (in the reference is equivalent to low portion of C-SYNC) after at least a gate clock cycle C1 (in the reference is equivalent to FX (IN)) during vertical blank period VB (in the reference is equivalent to low portion of C-SYNC) (See Fig. 12, items C-SYNC, STV (IN), from Col. 8, Line 56 to Col. 9, Line 3).

It would have been obvious to one of ordinary skill in the art at the time of invention to incorporate teaching of Taguchi et al. into ARA in order to drive the display (See Col. 1, Lines 6-8 in the Taguchi et al. reference).

Taguchi et al. teaches to generate the start vertical signals STV (See Fig. 12, items C-SYNC, STV (IN), from Col. 8, Line 56 to Col. 9, Line 3).

APA and Taguchi et al. do not show pausing output of CPV and OE until end of the vertical blank period VB.

Herman teaches to pause OE' until end of vertical blank period VB (See Col. 3, Lines 39-45).

It would have been obvious to one of ordinary skill in the art at the time of invention to pause output of CPV and OE until end of the vertical blank period VB as shown by Herman for OE' signal in APA and Taguchi et al. system in order to utilize the same data several times during the display operation (See Col. 1, Lines 10-12 in the Herman reference).

As to claim 6, APA teaches a method of processing signals of a timing controller of a liquid crystal display module, comprising the steps of:

(a) receiving a data enable signal DE which has a vertical blank period;

(b) decoding the data enable signal DE to generate a vertical synchronizing signal (See Fig. 3-4, items VSYNC, in description See from page 1, Line 27 to page 2, Line 6);

© generating a gate clock signal CPV which has a plurality gate clock cycles C1-Cn (See Fig. 3-6, item CPV, in description See page 2, Lines 4-24);

(d) after a rising edge or a falling edge of the vertical synchronizing signal generating a plurality of gate-on enable signals OE simultaneously according to the plurality of gate clock cycles C1-Cn of gate clock CPV (See Fig. 3-6, item OE, in description See page 2, Lines 4-24);

(e) wherein the start vertical signals STV includes a first start vertical signal STV1 to determine a start scan location of a frame; and a second start vertical signal STV2 to offset flicker and display brightness of the liquid crystal display (See Fig. 3-6, items STV1, STV2, in description See page 2, Lines 4-6).

APA does not show after a rising edge or a falling edge of the vertical synchronizing signal generating start vertical signals STV before the end of the vertical blank period VB after at least a gate clock cycle C1 during vertical blank period VB.

Taguchi et al. teaches after a rising edge or a falling edge of the vertical synchronizing signal (See Fig. 12, item C-SYNC) generating start vertical signals STV (See Fig. 12, item STV (IN)) before the end of the vertical blank period VB (in the reference is equivalent to low portion of C-SYNC) after at least a gate clock cycle C1 (in the reference is equivalent to FX (IN)) during vertical blank period VB (in the reference is equivalent to low portion of C-SYNC) (See Fig. 12, items C-SYNC, STV (IN), from Col. 8, Line 56 to Col. 9, Line 3).

It would have been obvious to one of ordinary skill in the art at the time of invention to incorporate teaching of Taguchi et al. into ARA in order to drive the display (See Col. 1, Lines 6-8 in the Taguchi et al. reference).

Taguchi et al. teaches to generate the start vertical signals STV (See Fig. 12, items C-SYNC, STV (IN), from Col. 8, Line 56 to Col. 9, Line 3).

APA and Taguchi et al. do not show pausing output of CPV and OE until end of the vertical blank period VB.

Herman teaches to pause OE' until end of vertical blank period VB (See Col. 3, Lines 39-45).

It would have been obvious to one of ordinary skill in the art at the time of invention to pause output of CPV and OE until end of the vertical blank period VB as shown by Herman for OE' signal in APA and Taguchi et al. system in order to utilize the same data several times during the display operation (See Col. 1, Lines 10-12 in the Herman reference).

As to claims 2, 7, APA teaches start vertical signals STV are generated after at least a third cycle C3 after start VB during the vertical blank period VB (See Fig. 3-6, items STV1, STV2, in description See page 2, Lines 4-6).

Response to Amendment

2. Applicant's arguments filed on 07-20-04 with respect to claim 1-2 and 6-7 have been considered but are moot in view of the new ground(s) of rejection.

Telephone inquire

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonid Shapiro whose telephone number is 703-305-5661. The examiner can normally be reached on 8 a.m. to 5 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 703-305-4938. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ls 12.02.04

VIJAY SHANKAR
PRIMARY EXAMINER